DESIGN FAQs

Frequently Asked Questions:

CLOCK REQUIREMENTS FOR DATA CONVERTERS

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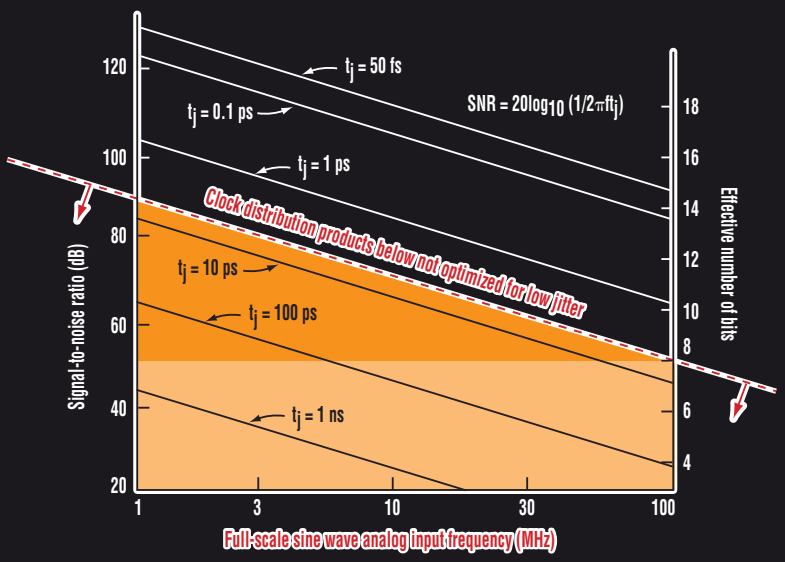
What's the relationship between jitter, phase noise, and signal-to-noise ratio (SNR) in data converters?

Clock jitter is a problem in data conversion because it introduces uncertainty (noise) into the conversion process. Jitter in the time domain is equivalent to phase noise in the frequency domain. Phase noise spreads some of the clock's power away from its fundamental frequency.

This is significant because sampling can be equivalent to mixing or multiplication in the time domain, which is equivalent to convolution in the frequency domain. Thus, the spectrum of the sample clock is convolved with the spectrum of the input signal. Also, because jitter is wideband noise on the clock, it shows up as wideband noise in the sampled spectrum. The spectrum is periodic and repeated around the sample rate. Thus, this wideband noise degrades the noise floor performance of the analog-to-digital converter (ADC).



2. This chart plots theoretical SNR and effective number of bits due to jitter versus input frequency for a number of jitter characteristics.

1. The encode signal is convolved with the analog input, so the clock spectrum (left) is expressed on the analog signal itself. Because the ADC is a sampled system, the wideband noise of the sample clock is also aliased back within the band of interest (right). This causes all of the wideband noise that enters the encode port to be aliased within the Nyquist band.

What equations can be used to analyze the effects of jitter/phase noise on converters?

To calculate the effect of phase noise on SNR, consider that a clock time delay is equivalent to a phase delay at a given frequency. In terms of noise power, this implies that phase noise in rms radians, σ_θ^2, equals ω^2_{clk} times σ_t^2, where σ_t is the phase jitter in rms seconds, and ω_{clk} is the clock frequency in radians/s. Thus, for any value of jitter error, a higher-frequency signal will have a greater phase error.

Phase noise defines the clock SNR by:

$$SNR_{clk}(dB) = -10\log \sigma_\theta^2$$

Assume a simple case in which the bandwidth of the clock jitter falls into a single Nyquist zone, and exclude quantization noise and thermal noise. In single-carrier systems, then, the SNR of a signal, f_0, sampled with a jittery clock is:

$$SNR_{sig}(dB) = 1/(4\pi^2\sigma_t^2 f_0)$$

In multicarrier narrowband systems, the SNR in decibels referenced to one of the carriers (dBc) would have the same form, but the sum of all the frequency terms would replace the f_0 term in the denominator. This is significant because it raises the quantization

and thermal noise floor. So in these applications, jitter may not contribute greatly to the overall SNR, and quantization and thermal noise may dominate.

But in wideband systems, assuming the data has zero mean and a flat spectrum uniformly distributed between two frequencies, f_L and f_H, it can be shown that:

$$SNR_{sig} = (1/\sigma_t^2) \times 3/(f_H^2 + f_H f_L + f_L^2)$$

What about converters operating above baseband?

Undersampled systems, such as those in which the signal frequency occupies one of the higher Nyquist bands, require clocks with much better phase jitter than baseband systems. This is because if the jitter is large enough, the noise caused by jitter can alias back in-band *(Fig. 1)*. In these applications, SNR limitations due to jitter can be determined by:

$$SNR(dB) = -20\log(2\pi f_{analog} t_{rmsjitter})$$

Where f_{analog} is the input frequency and t is the jitter. Given a frequency of operation and an SNR requirement, the clock jitter requirement can be determined using:

$$t_{jitter} = (10^{(-SNR/20)})/2\pi f_{analog}$$

Consequently, if jitter were the only limitation to converter performance, sampling an IF signal of 70 MHz while maintaining a 75-dB SNR would require a maximum clock jitter limited to 400 fs.

How is clocking a data converter different from clocking other digital applications?

The level of jitter or phase noise that can be tolerated is actually lower in the case of high-speed data converters than it is for very high-speed communications systems. For example, Sonet/SDH specs permit clock jitter on the order of a few picoseconds. But for a data converter operating at 100 Msamples/s with analog input frequencies of 70 to 200 MHz, jitter must be less than 1 ps *(Fig. 2)*.

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