Board decoupling using a standard methodology

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As Moore's Law has marched through the 1990s into the new millennium, each process node has brought a doubling of density with increased clock and data-transfer speeds and frequencies. Each node, however, also includes the nasty side effects of faster chip, board, and system di/dt transition-voltage noises, as well as signal jitter. To deal with these side effects, engineers need to know how to correctly bypass and decouple high-speed di/dt transitions to reduce noise that the system contains or radiates in some form of EMI.

To achieve this goal, it is important to devise a method of addressing the issues involved in picking and placing bypass and decoupling capacitors for high-speed digital chips, boards, and systems.

Finding the noise source

The purpose of decoupling a digital chip or board is to remove unwanted frequency noise from the system at any level. To accomplish this task, you must first look at the source or cause of the unwanted noise. In almost all instances, di/dt or ΔI noise is the source. For a digital chip or system, a change in the digital state of the chip or system from either a logic-zero state or a logic-one state brings about a current surge that causes a current-level change. Knowing di/dt or ΔI can help you find the amount of decoupling that a chip needs and then determine the system or board-level decoupling, but you first need to develop a method for finding ΔI:

$$I_{PER\ GATE} = \frac{V}{R_{TTL}} \text{ or } C\frac{dV}{dt_{CMOS}}.$$

EQUATION 1

Using **Equation 1** and a 74VHC1G04 chip, for example, with a gate capacitance of 3 pF, a dt of 1 nsec for t_R or t_P, and a maximum noise voltage of 50 mV:

$$\Delta I_{PER\ GATE} = 3\ pF\frac{50\ mV}{1\ nSEC} = 0.00375A.$$

EQUATION 2

The per-gate information is often unavailable, so a per-pin calculation works just as well. Each pin generally has a drive-cell macro behind it that you can treat as a pseudocell. Using a 74LVC04 as a step up in complexity, the results would be:

$$\Delta I_{PER\ PIN} = 5\ pF\frac{2.7V}{1\ nSEC} = 0.0135A,$$

$$\text{or } \Delta I_{PER\ PIN} = 5\ pF\frac{0.135V}{1\ nSEC} = 0.00068A.$$

EQUATION 3

The first number, 13.5 mA, is for current drawn for each full voltage switch per pin; the second number, 0.68 mA, indicates the voltage droop, 5%, that causes noise-current draw from across the power planes per pin, gate, or power bus. Therefore, ΔI for the whole chip equals ΔI times the six drive pins, or 81-mA, and the switching-noise (5% voltage droop) current is 4.1 mA for a 74LVC04.

Next, you need to determine the maximum power-bus impedance, because a digital system sees noise as voltage, or ΔI·Z=ΔV. Therefore, you now have

$$\Delta Z = \frac{\Delta V_{NOISE\ MAX}}{\Delta I},$$

EQUATION 4

which gives maximum impedance. From this **equation**, you can look for f_{PB}, the point at which $1/\omega C_D$ and ωL_B cross (Figure 1). At f_{PB}, the decoupling capacitors must begin working as high-frequency shorts and current supplies. The f_{PB} point indicates when impedance starts switching to an inductive impedance, which limits the responsiveness of the power bus to high-frequency power needs. The last parameter, ωL_D, is the shifted inductance line that the decoupling creates. Point f_{PD} is the place at which the inductance moves the system impedance back above the point at which current draw creates more voltage noise than is acceptable in the system. Z_{BUS} is the impedance of the power bus, which includes the power planes in a printed-wiring board.

Now that you know the origin of the remaining parameters, work toward C_D, which is the capacitance value that you need for the power/ground pairs on the chip that you are working to decouple. Using **equations 3** and **4**, you can calculate C_D from the following:

$$C_D = \frac{1}{2f_{PB}Z_{MAX}\pi}.$$

EQUATION 5

The last step is to make sure that C_D will work from f_{PB} to f_{PD} and is achievable for the needed high-frequency decoupling range.

Now, go back to the 74LVC04-chip example. The chip is a CMOS hex inverter. The di for a 74LVC04 at a V_{CC} of 2.7V has a 12-mA maximum output per driver from the data sheet. Assuming a 10 to 90% window, dv is 2.16V, and the assumed switching time is 1 nsec. Therefore, the minimum decoupling capacitance for the 74LVC04 is:

$$C_{MIN} \approx \Delta I \times \Delta T/\Delta V \approx \frac{72\ mA \times 1\ nSEC}{2.16V} \approx 33\ pF.$$

EQUATION 6

However, you need to take care of the voltage droop or noise that the driver current surge causes. So, the ΔV should be 50 mV for this example. This value gives you a minimum capacitance of:

$$C_{MIN} \approx 72\ mA \times 1\ nSEC/50\ mV \approx 1.44\ nF.$$

EQUATION 7

This one sample chip could be on a board with 20 or 30 chips—from a simple 74LVC04 to Pentium-

class chips with hundreds of pins or bond-out attachments. If more advanced software is not close at hand, a spreadsheet is the best way to obtain the total board capacitance and number of needed capacitors.

As a final example, work through the calculations for a generic PCI-X board with chips having well-defined parameters and a number of different main and support chips. The main processor chip is a 133-MHz PCI-X chip with a 3.3V I/O ring and 1.8V core, using a 40-MHz oscillator. Support chips are a 29LV040B EEPROM, dual low-dropout voltage regulator to supply 3.3 and 1.8V; a Palce16C8; one two-wire serial 24C32 EEPROM; and a CY37064VP44 CPLD. For each of these chips, you need to locate the current drive for each driver pin; determine the signal rise time, or Δt; and decide on the maximum noise voltage. Once you have chosen the decoupling capacitance, you can use the following equations to ensure that the impedance is not excessive and that the system does not have a resonance point:

$$Z_C = \sqrt{L/C}, \text{ and } f_O = \frac{1}{2\pi\sqrt{LC}}.$$

EQUATION 8

Table 1 covers the processor-chip board-decoupling parameters and per-chip board-decoupling capacitance needs.

So far, this article has focused on the lowest level (closest to the driver) or highest frequency of decoupling on a printed-wire assembly or circuit module—namely, the immediate quick-response current drawn for the chip at 1 MHz and greater frequencies, where t_R or t_F is 1 msec or less. However, bypass and decoupling need to occur at three levels of current-frequency draw for planned decoupling, with each of the levels requiring that the impedance be less than 1Ω for the best current-surge response and lowest noise or jitter characteristics at the chip and system levels. At the first level, the high-frequency quick-current surge associated with the digital-state and signal-I/O driver changes either on or off chip. The two other levels are the middle- and low-frequency ranges. Both ranges are resupply points to the next lower level of current-frequency bypass or decoupling.

Midfrequency component level

Designers generally view the midfrequency range of tens to hundreds of kilohertz as a board-level issue or intermediate current- and voltage-supply depot. The intermediate bypass capacitors supply the chip-level decoupling capacitors with their immediate-need surge-current resupply through relatively low-inductance paths. The midrange bypass capacitors tend to have an inductance path at least an order of magnitude larger than the inductance path between the chip-level decoupling capacitors and the chips they supply. This tendency results in a response time for the midrange bypass capacitance that is close to an order of magnitude higher than the response time of the chip-level decoupling capacitors, with capacitor values in the single- to low-double-digit microfarad range of values.

The midrange is at a chip level. So what is Δt? The PCI-X microprocessor chip has core, memory, and PCI-X operating blocks, each of which has a different Δt or operating frequency. The correct Δt is the slowest one. It gives the minimum capacitance that is large enough to pass all frequencies of concern in the midrange (Table 2).

Low frequency and power rails

The low-frequency, or bulk-decoupling, range is associated with the power-supply bus, which connects the system/board power supply to the system and onto the board through either edge

fingers or cable/wire connections. This bus usually has noise from a few hertz to 10 or 20 kHz, with a voltage and current ripple that you must consider when specifying parts. At this level, the value of capacitance is in either the hundreds or the thousands of microfarads.

Also at this level, you want to make sure that the power-bus impedance is low enough for the total board current draw (ΔI_{TB}) and the maximum voltage-noise budget. To determine this information, you need to know X_{MAX}, which is equal to $\Delta V_{NOISE\ MAX}/\Delta I_{TB}$. Once you know the maximum impedance, you need to estimate, calculate, or measure inductance for the power-supply rail leading up to the board. You can use this power-rail inductance, L_{PS}, to find the total capacitance the board needs to determine X_{MAX}. You can also use the L_{PS} to calculate the power-rail frequency needed to arrive at the total board capacitance.

Results

Tables 3 , 4 and 5 show the results for high-, middle-, and low-frequency capacitance calculations on the PCI-X HAB (host-adapter-bus) board. At high frequencies, the PCI-X microprocessor chip needs 11 0.01-µF capacitors. In practice, you could further divide these capacitors into values of 0.01 µF, 1000 pF, and 110 pF, to give a number sufficient for one decoupling capacitor per two power/ground-pin pairs. This step minimizes the via and plane inductance in an attempt to keep the impedance from the capacitors to the power pin as far below 1Ωas possible. However, you must also stay within the necessary amount of capacitance and use a minimal number of capacitors. Three values help hold the response curve as flat as possible across the high-frequency spectrum. You should not place the capacitors next to each other in a parallel arrangement, because doing so dampens the effectiveness of the very-low-value capacitor. One practical side benefit of knowing the correct amount of capacitance is that you can avoid overusing capacitors, which can open board-routing channels around large chips and reduce via count through power and ground planes.

You then need to calculate the total board bulk capacitance. Make sure that high, middle, and low ranges add up to a total that will give the capacitance value that will deliver the needed impedance for X_{MAX} for the power-supply rail: $X_{MAX}=\Delta V_{NOISEMAX}/\Delta I_{TB}$: From Table 5, $\Delta V_{NOISEMAX}$=50 mV, and ΔI_{TB}=1.64A. X_{MAX}=0.030Ω, and L_{PS} is 200 nH. So, $f_{PS}=X_{MAX}/2\pi L_{PS}$=0.030/2π200 nH=24 kHz. Therefore, $C_{TB}=1/2\pi f_{PS}X_{MAX}$=220 µF.

The total capacitance from tables 3 , 4 , and 5 is 1.62 µF. So, the board needs 220 µF for bulk capacitance to pull the power-supply-rail impedance up to 0.030Ω. This value is large for a board that is the size of a normal PCI plug-in card. You should therefore review issues that can affect the value for the bulk capacitance if this amount of bulk decoupling will be a problem.

A ΔV, voltage droop, or jitter factor of 50 mV might indicate that the analysis is too stringent, so you should look at other ways to lower the power-supply-rail inductance to reduce the bulk decoupling to a smaller value. Changing ΔV to 100 mV moves C_{TB} to 54 µF. This change, however, makes the invalid assumption that only this card is on the PCI power rail. You can achieve the same effect by reducing the power-supply-rail inductance to 100 nH.

The key parameter for specifying a more appropriate amount of decoupling capacitance is keeping the current-supply bus impedance between the bulk capacitors and the power supplies below 1Ω. The lower the impedance, the better your chance of minimizing the voltage noise or jitter that the 0Ω, nonideal power-bus impedance generates.

A critical topic that this article does not cover is the impedance between the decoupling/bypass-capacitor placement and the attachment methodologies. The best capacitor-attachment approach is to use surface-mount components with vias in pads to create small inductance-loop areas and, thus,

small inductance values to minimize the impact on path impedance.

Read more about it

This article makes many assumptions and simplifications for developing a workable approach to finding the value of decoupling capacitance at the levels that most often exist on a pc-board assembly. For more precise details and information, please see the following sources:

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