CAD oriented study of Polyimide interface layer on Silicon substrate for RF applications

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Abstract: Polyimide interface layer on standard silicon substrate extends the use of silicon for RF applications and is also compatible with the present CMOS technology. This paper investigates the characteristics of the microstrip lines patterned on polyimide interface layer up to 40 GHz. The limitation of lossy silicon substrate can be overcome by this approach. The full wave analysis of the microstrip line has been carried out using CAD tool. Also the non-ideal ground plane effects along with the concept of thicker bottom metallization below polyimide have been demonstrated to have lower losses.

Index Terms: Polyimide, Silicon substrate, attenuation, conductor loss, microstrip lines

1. Introduction

Device miniaturization and the use of hetero-structures (Si-Ge-Si) overcome the limitation of silicon based transistors in the microwave and millimeter wave applications. This technology demands the integration of passive RF circuits on the same chip. Further, for cost-effective and high volume production at these frequencies, standard CMOS integrated circuit processing is desired consisting of RF/digital/analog functions on the same chip. However, traditionally microwave circuits realized on the low resistivity silicon (LRS) substrates i.e. CMOS grade Si wafers, exhibits higher losses.

This problem can be alleviated by using high resistivity silicon as suggested by Buechler et al[1]. But high resistivity silicon (HRS) not only is costlier but exhibits high dielectric loss. As at high frequencies, the dielectric behavior of the silicon substrate, assuming to be resistive, is no longer valid below the dielectric relaxation frequency defined by

$$fc = \frac{1}{2\pi\varepsilon_{Si}\rho_{Si}} = \frac{1}{2\pi R_{sub} C_{sub}} \qquad (1)$$

where R_{sub} and C_{sub} are the resistance and capacitance of the substrate and ρ_{Si} and ε_{Si} are the resistivity of the substrate and permittivity of the substrate, respectively.[2]This relation also shows strong dependency of the doping on the fc. Alternately, dielectric layer such as polyimide can be used on top of the CMOS grade substrate for the realization of the low loss microwave components. Both microstrip and coplanar waveguide transmission lines exhibit low attenuation in such circuits.[3] The reported structures are filters, couplers, patch antennas etc.[4,5]However, not much attention was

paid for characterization and loss mechanisms associated with these interface layers. Also the polyimide used so far by the researchers (PI-1111) is not commercially available. Hence, a proper characterization and validation of the interface layer, with the commonly available polyimide has to be carried out in this regime.

This paper presents the characterization of microstrip lines on the polyimide interface with technique for further improvement in the line losses. Enhanced spectral domain method (SOE) is used, in this analysis, to generate strip characteristics. The polyimide chosen in this study is PI - 2525 from Hitachi Chemicals with the maximum thickness of 13μm and having permittivity of 3.3 along with dissipation factor of 0.02. [9]

2. Theoretical Background

The material taken for the analysis is the silicon substrate having typical conductivity of 20 S/m with the thickness of 675 μm. The electric field at the bottom plate is considered to be lesser than the top. The attenuation constant at the bottom plate can be found using

$$\alpha = \omega\sqrt{\frac{\mu\varepsilon}{2}}\left(\sqrt{1+\frac{\varepsilon''}{\varepsilon'}}-1\right) \text{ where } \varepsilon' = \varepsilon_r\varepsilon_0 \text{ and } \varepsilon'' = \frac{\sigma}{\omega\varepsilon} \qquad (2)$$

This relation shows considerable electric field at the bottom surface compared to the top which can excite substrate modes and can affect the frequency of operation. So a ground plate at the bottom of the polyimide layer can minimize the interaction of the electric field with the lossy silicon substrate.

3. Characterization of the Microstrip Line realized on Polyimide interface layer

Four variants of the circuits have been investigated and compared in terms of effective permittivity, attenuation loss, conductor loss and dielectric loss. The width of the line and height of the substrate is assumed to be constant. The metallization thickness of the line is kept as 1μm for foundry specific reasons in all these cases. It is seen that effect of the resistivity of the substrate is minimum on the primary parameters of the lines. The first variant (case-1) is realized by depositing polyimide directly on the silicon substrate as shown in Fig 1.

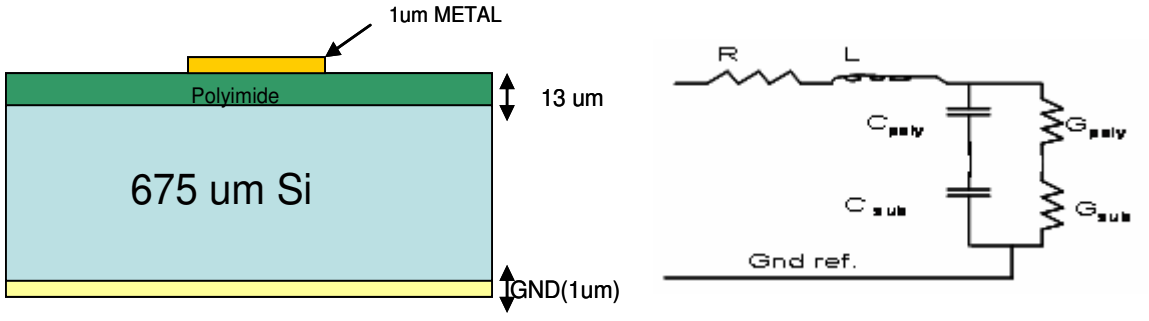

Fig 1: Interface layer of polyimide on Si substrate and equivalent circuit

This approach gives more dielectric losses along with higher effective permittivity which is not suitable for patch antenna realization as discussed in section 3.1.

In the second variant (case-2) metal is deposited beneath polyimide as shown in Fig 2. This avoids the electric field concentration beneath the polyimide and reduces the effect of lossy silicon substrate.

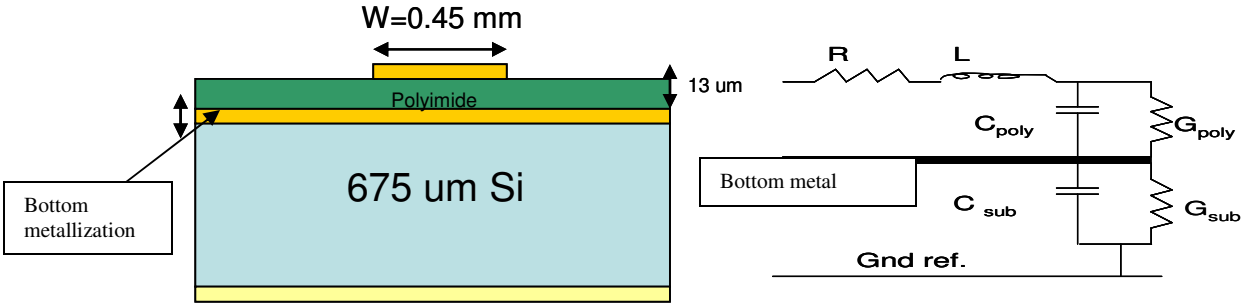

Fig 2: The deposition of metal layer on the bottom of polyimide and its equivalent circuit

In the third variant (case-3), the thickness of the bottom layer is varied and its effect on the line characteristics studied. This is shown in the Fig 3.

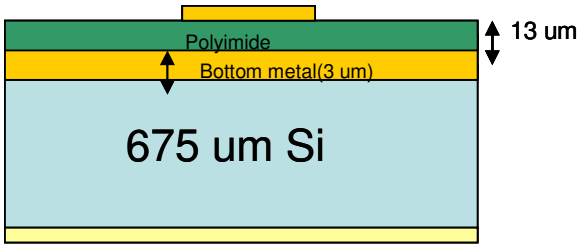

Fig 3: (a) Variation in the bottom metal thickness

In the fourth variant (case-4) the effect of the ground plane is studied taking both ideal and non-ideal characteristics. A ground metallization beneath silicon is provided to facilitate grounding as well as generation of ground reference for practical measurements.

3.1 Effective Permittivity variation with frequency

The fig 4 shows the variation in effective permittivity ,which decreases with frequency at around 30 GHz. Verma et al [6] has given concept of virtual permittivity but could not explain the behavior as depicted around 30 GHz. This phenomenon can be attributed to the lowest order transverse microstrip resonance given as

$$fc = \frac{c}{\sqrt{\varepsilon r(2w + 0.8h)}} \qquad (3)$$

which comes out to be around 27 GHz for h=.675 mm, w=.45 and εr =11.8. Also the lowest order TM mode limitation given as [7]

$$f_{TM}\,(\text{GHz}) = \frac{75}{h\sqrt{\varepsilon r - 1}} \approx 30\ \text{GHz}\ .$$

These effects, combined with dispersion phenomena are reducing the overall permittivity at higher frequencies.

Also the normalized impedance for the case shown in fig 1 is also plotted and marked as B in Fig 4.

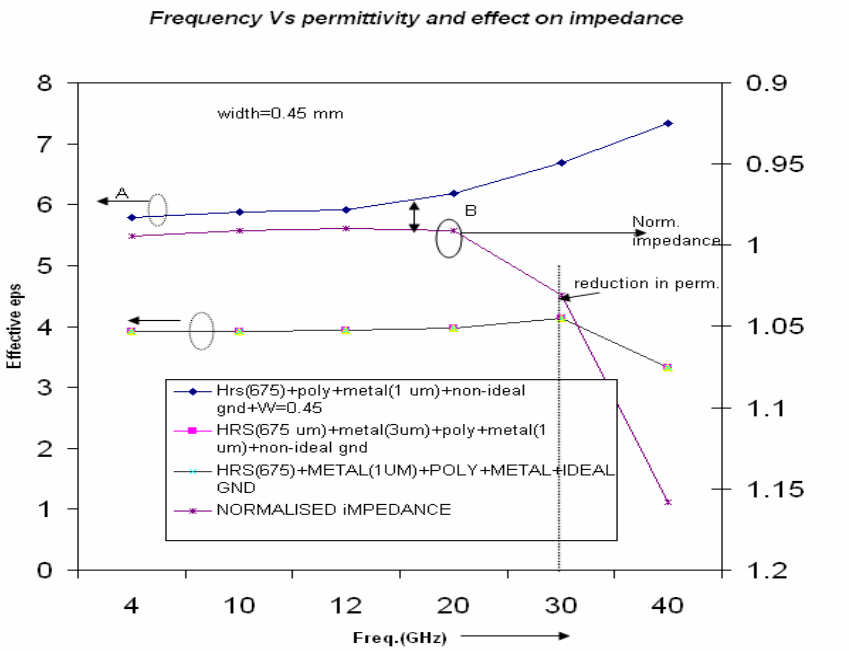

Fig 4: Change in effective permittivity with frequency.

3.2 Attenuation variation with frequency

Total attenuation in microstrip line is the combination of the loss contributed by conductor, dielectric, radiation and surface waves. The effect of bottom layer beneath polyimide as well as effect of thickness can be understood from the fig 5 and 6 respectively. Fig 5, clearly demonstrates that up to 30 GHz, the higher thickness of the bottom plate reduces the attenuation, considerably, as can be seen from the plot of conductor loss shown in Fig 6. The skin depth which is around 0.39 µm at 4 GHz falls to 0.063 µm at 40 GHz. The top metallization thickness is taken to be 1µm (foundry specific) and can be considered well above practical limits (metallization thickness to be at least three skin depth at operating frequencies). Further the insertion of the ideal ground plane reduces the loss further which is also shown in the plot. Fig 7 shows the comparison of dielectric loss contribution of bottomless polyimide (case-1) along with bottom plate (case 2-3).The variation comes out to be 25% at lower

end of the frequency. Also, no variation of the dielectric loss is seen with the bottom layer thickness. All these cases are studied by taking tanδ=.01 for silicon and tanδ=.002 for polyimide.

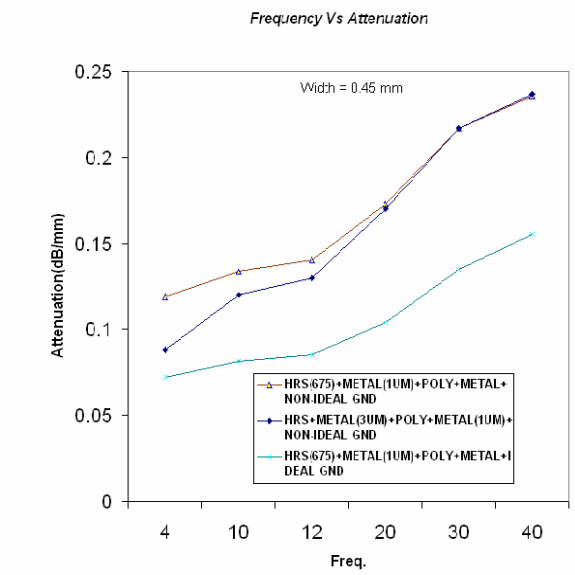

Fig 5: Attenuation loss variation

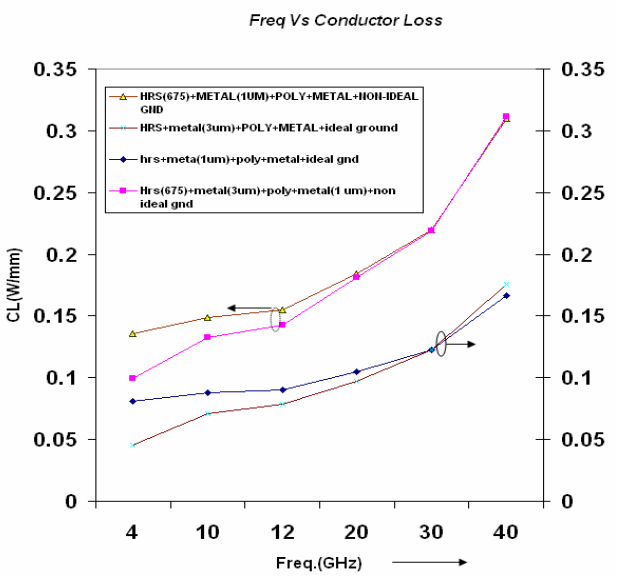

Fig 6: Conductor Loss variation

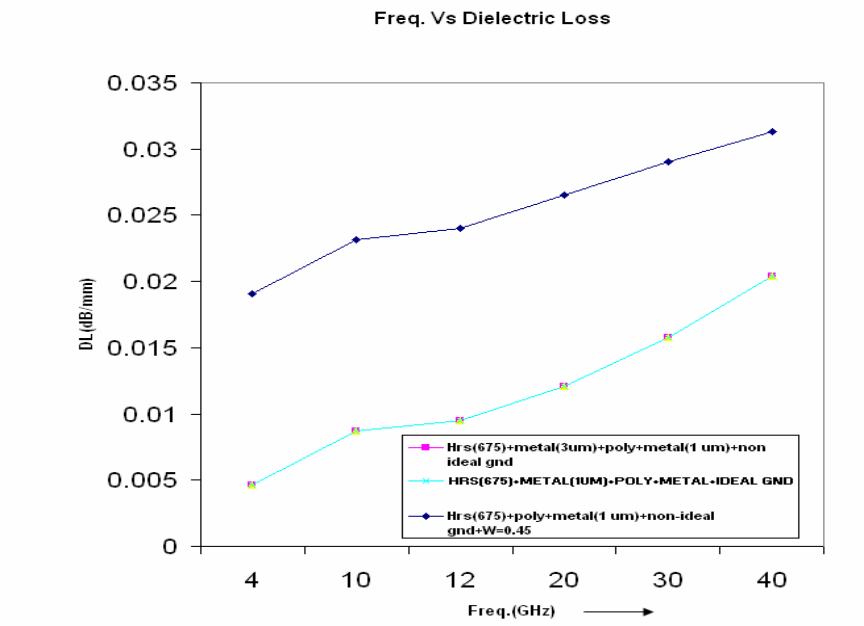

Fig 7: Dielectric Loss variation with frequency [loss comparison with case1]

The above observed phenomena can be attributed to dispersion at which the quasi-static assumptions are inadequate and a full wave solution allowing for complete matching at the dielectric-air interface is needed. This is done using the 2D EM field theory based full-wave simulator MMICTL [8] using the enhanced spectral domain method.

Another major characteristic in a transmission line is the concept of propagation delay. Propagation delay is the major criteria when pulse signal is carried by microstrip lines.

$$\tau_d = \frac{1}{\upsilon_p} = \frac{\sqrt{\varepsilon eff}}{c} = \frac{1}{c}\sqrt{\frac{C_{sub}}{C_{air}}} \text{ s/m} \qquad (4)$$

The delay of around 200 ps is necessary for the high speed samplers and oscilloscope working with pulse propagation. Delay relation is directly proportional to the effective permittivity and can be made application specific by the concept of loading which in turn increases capacitance resulting in increased delay, as shown in eq.4.

4. Conclusion

This paper investigates the characteristics of the microstrip lines on polyimide interface layers and can be implemented on CMOS grade silicon substrate for RF applications. The concept can be used for the microstrip based realization of passive RF structures and a step forward in the integration of RF and CMOS circuitry on the same chip. Microstrip is a preferred medium compared to CPW due to higher Q achievable with this topology. The passive circuits on microstrip can be easily realized up to millimeter wave frequencies using this concept. Authors propose the use of thicker layer beneath polyimide for minimizing the losses. The thicker bottom layer reduces the attenuation by more than 10% up to around 20GHz but at higher end the effect subsidizes due to leakage in Si substrate and associated loss. The losses as shown can be further reduced if ideal ground plane properties have been incorporated. Thus, though polyimide has shown great potential for use in RF applications, its unfavorable viscoelastic properties have to be overcome by taking due care in fabrication. Future work involves the investigation of the coupled lines approach along with the closed form expression for a close match with the practical results. The effect of the shielding enclosure also needs to be taken into cognizance. Further studies on modeling are being planned.

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