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A phase-locked loop (PLL) is a feedback system whose function is to force a voltage-controlled oscillator (VCO) to be coherent with a certain reference frequency. By "coherent" is meant highly correlated in both frequency and phase.

Heuristically, the loop operation is relatively simple (see Figure 1). The phase detector compares the instantaneous phase difference between the reference oscillator and the VCO, then puts out a voltage (or current) proportional to the error. The loop filter then amplifies the error and drives the VCO to reduce the error. The action of the loop is to slew the frequency of the VCO until the phase error is zero and the two oscillators "track." Thus, this elementary form of the PLL is often called a "tracking filter." Looking a little closer at the action of the loop, let it be assumed that at some point the VCO is leading in phase relative to the reference oscillator. The phase detector loop filter will respond by supplying a voltage to the VCO such that the VCO's output frequency will decrease. As the VCO's frequency lowers, the phase lag between the reference oscillator and the VCO will decrease. This is shown more clearly in the timing diagram of Figure 2. This process continues until the VCO is in phase with the reference and has the correct control voltage to maintain it at the same frequency as the reference oscillator.

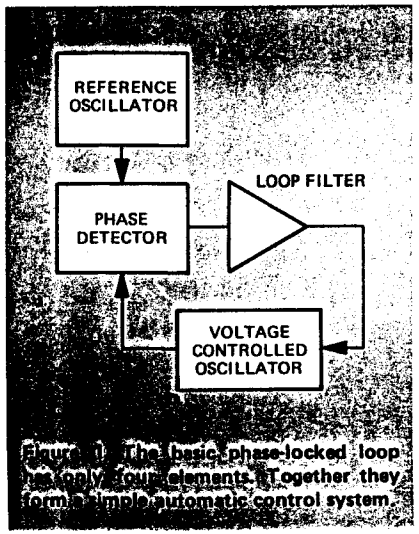



Figure 1. The basic phase-locked loop has only four elements. Together they form a simple automatic control system.

Although phase-locked loops and phase-tracking systems have been in existence for quite some time, the movement to incorporate them into microwave designs has been relatively slow. Some of the reasons for this include: (1) Since spectral crowding is just beginning to become a major problem (relative to the HF and UHF bands), long-term stability and absolute frequency accuracy have not been primary design goals. (2) Phase-locked loops incur additional expense because they require extra microwave components which add to the overall system cost. These expensive components typically include a broadband directional coupler, a broadband mixer (usually a biased or "Starved LO" type) and an IF amplifier. (3) Radar and digital communications had not yet reached the point at which short-term stability had become a problem. (4) Reliability was a problem. The old phase-locked loops used mixers as phase detectors, which led to problems of "false locking" and other conditionally-stable modes.

There was also the major acquisition problem of getting the loop to a locked condition from an unlocked condition. The pull-in range for a phase-locked loop using a mixer as a phase detector was relatively short, and even when the signal was within the pull-in range, the loop was generally very slow in pulling the signal into phase lock. If the signal was outside of the pull-in range, the loop would never lock. To combat the acquisition problem, complex analog circuitry was developed that swept the VCO until the loop locked. This did very little to further the reliability of the loop.



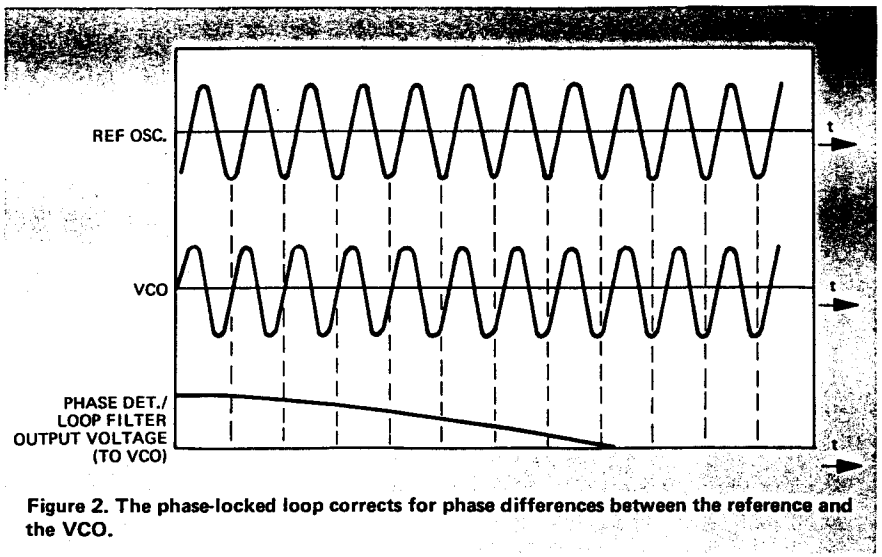



**Figure 2. The phase-locked loop corrects for phase differences between the reference and the VCO.**

Today, however, more and more designers are using phase-locked techniques to improve system performance. The availability of phase-locked loop components, boosted by the Citizen's-band boom, has made phase-locked loop designing almost a cookbook procedure.* This article deals with those cases where the cookbook formulas just do not work and valuable time must be spent modifying the design to make the circuit operate properly. "Transportation Lag," or time delay in the loop is often the problem; learning to design around it can eliminate much frustration and many wasted manhours.

## Mathematical Description

The model for the PLL is shown in Figure 3. To understand how this model functions, an input signal of the form

$$A_R \text{ Sin } (\omega_R t + \phi_i)$$

and a VCO output signal

$$A_o \text{ Sin } (\omega_R t + \phi_o)$$

will be used.

Here, $\phi_i$ is the input reference phase, $\omega_R$ is the reference frequency in radians/sec and $\phi_o$ is the VCO output phase relative to the reference frequency. To find an expression for $\phi_o$, it is assumed that the center (zero correction voltage) frequency for the VCO is $\omega_R$ and that the deviation from that frequency is given by

$$\Delta\omega = K_o v_o = \frac{d\,\phi_o}{dt}$$

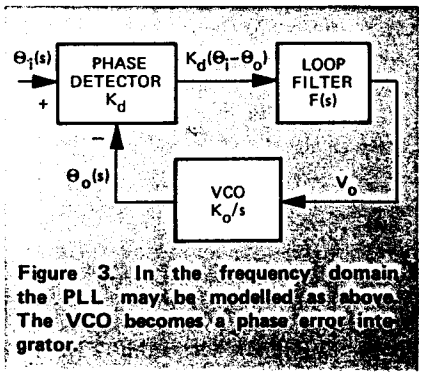



Figure 3. In the frequency domain the PLL may be modelled as above. The VCO becomes a phase error integrator.

*See, for example, Gardner, F. M., *Phaselock Techniques*, or the Motorola *Phase-locked Loop Systems Data Book*.

where $K_o$ is the VCO constant in units of radians/second per volt and $v_o$ is the input control voltage to the VCO. Thus, $\phi_o$ is given by

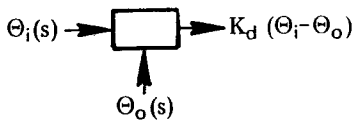
$$\phi_o = \int_{-\infty}^{t} K_o\, v_o\, dt$$

or

$$\Theta_o(s) = \frac{K_o\, V_o\, (s)}{s}$$

in the frequency domain. The VCO is modelled as an integrator in the model of Figure 3.

Meanwhile, the phase detector is modelled as




where $K_d$ is a constant with dimensions of volts/radian.

Starting at the phase detector, the signal may be followed around the loop so that

$$K_d\ (\Theta_i - \Theta_o) \cdot F(s) \cdot \frac{K_o}{s} = \Theta_o. \quad (1)$$

And, solving this for

$$\frac{\Theta_o}{\Theta_i},$$

the transfer function of the loop is

$$\frac{\Theta_o}{\Theta_i} = \frac{K_o K_d F(s)/s}{1 + K_o K_d F(s)/s} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)}. \quad (2)$$

The transfer function of the linearized PLL model describes the behavior of the PLL as a function of the frequency of the input phase variations. This frequency should not be confused with signal frequencies. For example, if the input to a tracking PLL is a signal which is phase modulated at a rate $\omega_m$, the PLL (assuming it has a bandwidth greater than $\omega_m$) will track the phase variations and will modulate the VCO at a rate $\omega_m$. As will be discussed later, the effect is that the VCO will have upper and lower phase modulation sidebands at $\omega_c + \omega_m$ and $\omega_c - \omega_m$, where $\omega_c$ is the center frequency of the VCO. This means that phase variations occuring at a rate $\omega_m$ translate to sidebands at an offset $\omega_m$ from the carrier.

It should be noted that the order of the loop is equal to one plus the order of the loop filter, F(s). For a first-order loop, F(s) = $K_f$ = constant and

$$\frac{\Theta_o}{\Theta_i} = \frac{K_o K_d K_f}{s + K_o K_d K_f}. \quad (3)$$

This has a simple first-order roll-off with a corner frequency of $\omega_a = K_o K_d K_f$, which means that the VCO's output phase will track the reference phase out to about $\omega_a$. This is an important consideration for microwave oscillators. Figure 4a shows an unstabilized YIG oscillator with a typical noise spectrum and a crystal reference oscillator multiplied up to the microwave region. The phase noise of the PLL output is a composite of the multiplied-up reference phase noise and the free-running VCO phase noise. Within the loop bandwidth ($\omega_a$), the output will track the reference phase noise, since the PLL provides rejection to the VCO phase noise. Outside the loop bandwidth, the output phase noise will be that of the free-running VCO. As shown in Figure 4a, the best phase noise performance will be achieved when the loop bandwidth is set equal to the crossover frequency between the multiplied-up reference phase noise and the free-running VCO phase noise. Not only does the PLL give better phase noise, it may also give better long-term stability (see Figure 4b), since it can be phase locked to a reference which typically has excellent long-term drift characteristics.

Returning to the first-order loop, notice that if the reference oscillator takes a step change in frequency (or if the center frequency of the VCO changes), the phase detector is required to have a constant error of

$$\epsilon = \frac{2\pi\Delta f}{K_o K_d K_f}$$

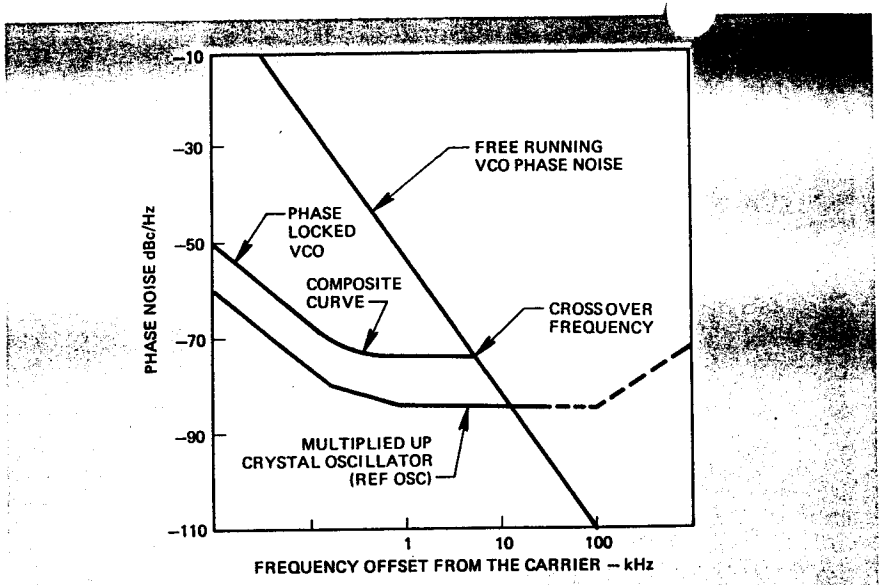



**Figure 4. The use of a phase-locked loop improves phase noise.**

to supply the required offset to the VCO.

In many types of digital phase detectors, this error results in pulses at the reference frequency getting on the VCO, and generating sidebands. In analog phase detectors, this can limit the pull-in range or cause distortion of detected FM. One way of avoiding this problem is to use a second-order loop by letting

$$F(s) = \frac{K_f\,(s+a)}{s}.$$

One possible implementation of this transfer function is shown in Figure 5.

This second-order loop has infinite gain at DC and, therefore, drives the steady-state phase error, $\epsilon$, to zero. The transfer function for this loop is

$$\frac{\Theta_o}{\Theta_i} = \frac{K_o K_d K_f\,(s+a)}{s^2 + K_o K_d K_f\,(s+a)} \qquad (4)$$

$$= \frac{K_o K_d K_f (s+a)}{s^2 + K_o K_d K_f s + K_o K_d K_f a}.$$

Putting the denominator in the standard form of

$$s^2 + 2\,\delta\,\omega_n s + \omega_n{}^2$$

where $\delta$ is the damping factor and $\omega_n$ is the natural frequency of the loop,

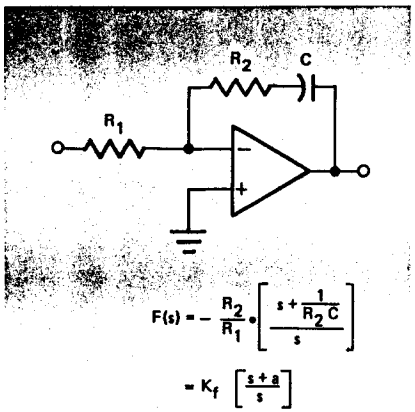



**Figure 5. Possible implementation of the second-order loop technique.**

gives

$$\delta = 1/2\sqrt{\frac{K_o K_d K_f}{a}}$$

and

$$\omega_n = \sqrt{K_o K_d K_f a}$$

as design equations.

## Onward to Synthesizers

Thus far, only an ideal phase-locked loop of the tracking-filter type has been discussed. While this type of loop makes an excellent example to demonstrate how the loop works, its applications are rather specialized and of narrow scope, since the input and output frequencies are the same. The more common case, especially at microwave frequencies, is one where it is desired to lock the frequency of an oscillator to an offset frequency from another signal. It may, for example, be necessary to stabilize a YIG oscillator to a fixed offset from a standard cavity oscillator, or to force two sweepers to track with a fixed (or programmable) offset, or to stabilize a receiver's LO to some standard crystal oscillator. To illustrate the action of a more general problem, a simple microwave synthesizer such as shown in Figure 6A may be considered.

The stable frequency for the loop is derived by the equation $f_o = f_1 + N \cdot f_r$. If $f_o$ is greater than the stable frequency, then $f_{IF} = f_o - f_1$ will be greater than $N \cdot f_r$, and $f_{IF}/N = f_o$ will be greater than $f_r$. The combination of phase detector/frequency discriminator and loop filter will then produce a correction voltage to lower $f_o$.

It should be noted that the frequency $f_o = f_1 - Nf_r$ is not a stable frequency even though it produces an IF of $N \cdot f_r$. This is because a perturbation on the VCO, which causes $f_o$ to increase from the value $f_1 - N \cdot f_r$, will result in a VCO correction voltage which will further increase $f_o$. Thus, if the initial perturbation increases $f_o$, the loop will be driven to $f_o = f_1 + Nf_r$

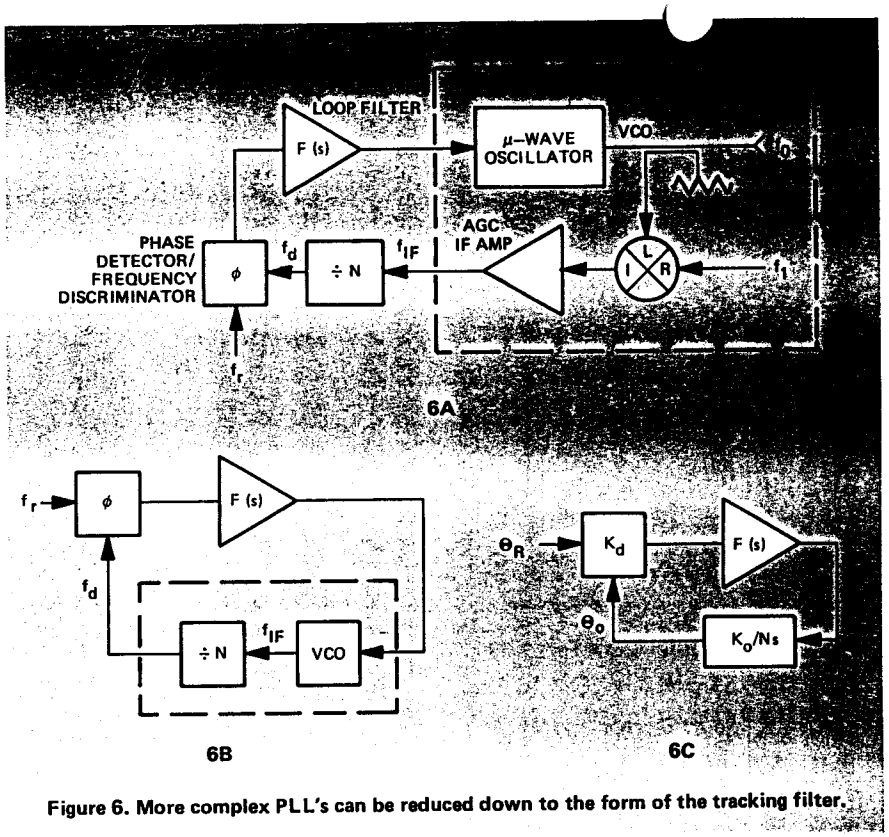



**Figure 6. More complex PLL's can be reduced down to the form of the tracking filter.**

(a stable point), but if the initial perturbation decreases $f_o$, the loop will "latch" with $f_o$ at its lowest value.

Because $f_o$ tracks $f_1$, it follows that if $f_1$ has FM (within the bandwidth of the loop) or drift associated with it, $f_o$ will track and will, therefore, have the same FM and drift. But, since $f_o$ also tracks $N \cdot f_r$, frequency or phase variations in $f_r$ will be magnified by a factor of N. Thus, if $f_r$ changes by 1 Hz, and N = 5000, the output, $f_o$, will change by 5 kHz. Even though the reference frequency comes from a very stable crystal oscillator that won't vary anywhere near 1 Hz, the existence, for example, of 60 Hz FM sidebands at -90 dBc on the reference will result in sidebands on the output, $f_o$, at -16 dBc.

### Multiplying Noise

Phase modulation sidebands are increased by an amount 20 log N when the carrier frequency is multiplied by a factor N.

Considering a signal

$$v(t) = A \sin [\omega_c t + \Delta\theta \sin \omega_m t]$$

where A is the signal amplitude,
$\omega_c$ is the carrier frequency,
$\omega_m$ is the modulation frequency,
and $\Delta\theta$ is the peak phase deviation due to the modulation,

if $\Delta\theta << 1$, then $v(t)$ can be approximated as

$$v(t) \cong A \sin \omega_c t + A(\cos \omega_c t)(\Delta\theta \sin \omega_m t)$$
$$\cong A \sin \omega_c t + A\frac{\Delta\theta}{2} \sin (\omega_c+\omega_m)t - A\frac{\Delta\theta}{2} \sin (\omega_c-\omega_m)t.$$

The signal $v(t)$ thus consists of a carrier and an upper and lower sideband whose amplitudes are a factor

$$\frac{\Delta\theta}{2}$$

below the carrier amplitude. In terms of signal power, the single sideband-to-carrier power ratio is

$$\left(\frac{\Delta\theta}{2}\right)^2.$$

If the signal $v(t)$ is passed through a frequency multiplier, the output frequency can be expressed as

$$v'(t) = A \sin [N\omega_c t + N\Delta\theta \sin \omega_m t].$$

Again, if $N\Delta\theta << 1$, then by a similar argument, $v'(t)$ can be resolved into a carrier and an upper and lower sideband:

$$v'(t) = A \sin N\omega_c t + A\frac{N\Delta\theta}{2} \sin (N\omega_c + \omega_m)t - A\frac{N\Delta\theta}{2} \sin (N\omega_c-\omega_m)t.$$

Now the single sideband-to-carrier power ratio can be seen to be equal to

$$\left(\frac{N\Delta\theta}{2}\right)^2.$$

Therefore, the effect of the multiplier on the single sideband-to-carrier power ratio is to increase it by a factor $N^2$. Expressed in decibels, this would be 10 log $N^2$ or 20 log N.

Similar arguments can be used if the phase modulation is a random noise signal instead of a discrete signal.

## Getting Back to Basics

The design of the loop shown in Figure 6A differs only slightly from the design of the tracking filter discussed previously. The differences are more easily discussed in stages until the loop takes the form of a tracking filter. The dashed area in Figure 6A, which includes the oscillator, mixer, $f_1$, and the IF amplifier, may be replaced by a new VCO that has an output frequency of $f_{IF}$, whose center frequency is $N \cdot f_r$, and that has the same tuning constant as the original oscillator. This leaves the block diagram as shown in Figure 6B.

It can now be seen that the only difference between the tracking filter and Figure 6B is the divide-by-N stage. However, the VCO and the divide-by-N stage can be combined into an equivalent VCO. If this is done, the equivalent VCO will have a VCO constant of $K_o' = K_o/N$ radians/second/volt. Thus, if a one-volt correction voltage would move the output oscillator (in Figure 6A) $\Delta f$, $f_d$ would move only $\Delta f/N$. Figure 6C shows the reduced block diagram. The design procedure is the same as for the tracking filter except that $K_o'$ is used in place of $K_o$.

## Transportation Lag

In most narrowband applications, the design equations function properly and the PLL operates effectively. But, when SAW filters are used in the IF and/or when the high-speed divider is dividing by a number large enough to create a phase shift that is appreciably significant compared to that of the phase shift due to the loop components, then time delays can become a problem. SAW filters make use of the much slower propagation rate of acoustic versus electromagnetic waves and, therefore, have inherently long group delays. High-speed dividers give one output pulse for every N periods of the input, such that if the input frequency is changed suddenly, the output will be delayed by $N \cdot T_i$ seconds, where $T_i$ is the period of the input signal. For example, if N = 5000 and $T_i$ = 2 nsec (500 MHz), the delay is 10 microseconds.

To understand how these time delays affect the performance of the PLL, it should be noted that a time delay of $\tau$ seconds may be represented in the frequency domain by $e^{-sT}$. This function has unity magnitude (gain) at all frequencies, but has a phase shift which changes linearly with frequency. Since engineers view stability in different ways, several of these ways will be discussed. Figure 7 shows a Bode plot of a typical second-order PLL before and after adding time delay. T(s) is the open-loop transfer function. The ideal second-order loop is unconditionally stable, and has a finite phase margin and an infinite gain margin, since the phase shift never reaches 180°. (Since the closed-

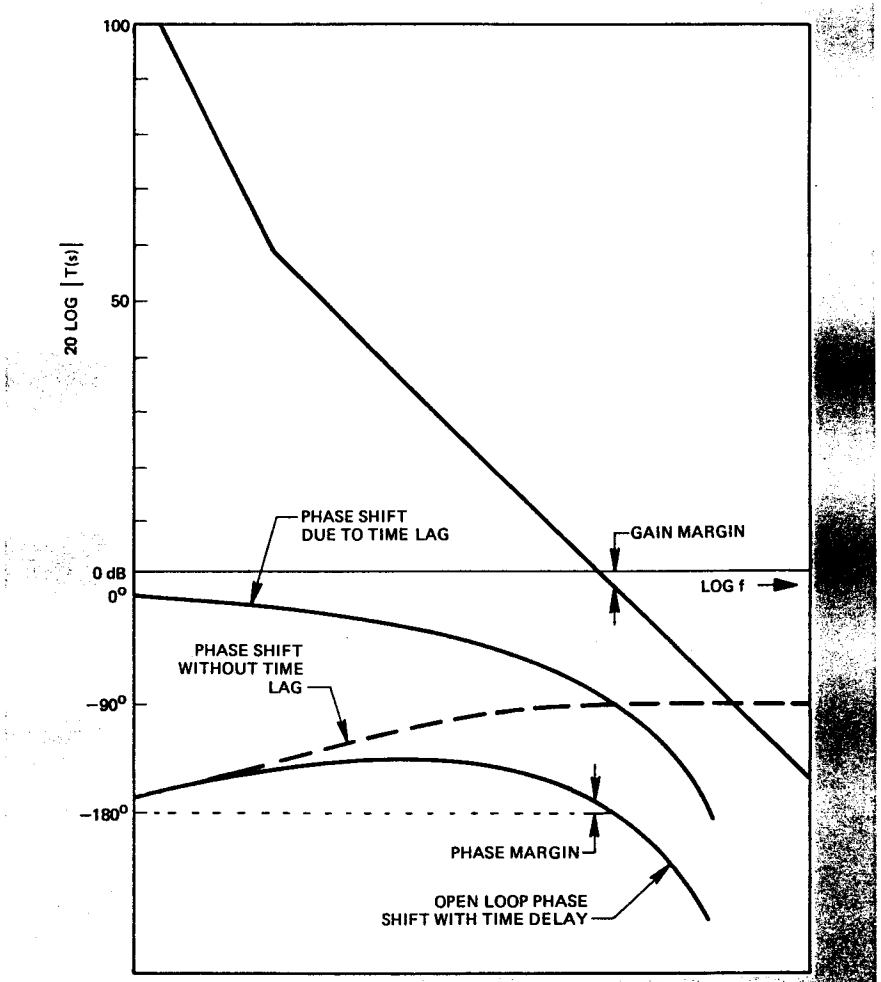



**Figure 7. This Bode Plot shows how time delay (transportation lag) reduces the phase margin.**

loop system will oscillate when $|T(s)| = 1$ and $\angle T(s) = 180^\circ (2k+1)$, the phase margin is defined as $180^\circ - \angle T(s_1)$, where $s_1$ is such that $|T(s_1)| = 1$. Gain margin is defined as 20 log $|T(s_2)|$, where $s_2$ is such that $\angle T(s_2) = (2K+1) \cdot 180^\circ$). As can be seen in Figure 7, the effect of the time delay is to reduce the phase margin and gain margin.

Another method of evaluating the loop performance is to examine the Nyquist Plot, an example of which is shown in Figure 8. The Nyquist Plot is a polar plot of T(s), such that the point $1\angle 180^\circ$ (minus one) is the critical point. The closer T(s) comes to the critical point, the more peaking and ringing there is in the closed-loop system. If the minus-one point is enclosed, the closed-loop system will be unstable.* The time delay tends to shift the Nyquist Plot clockwise and, therefore, closer to the critical point. This causes the gain of the closed-loop transfer function to peak, and results in ringing in the step response and noise peaking in the spectrum. Examples of the type of noise peaking are shown in the spectrum analyzer photos in Figure 9. Figure 9A shows noise peaking about 20 kHz away from the carrier, while Figure 9B shows the noise peaking removed; in this case, by reducing the bandwidth by a factor of 1.4.

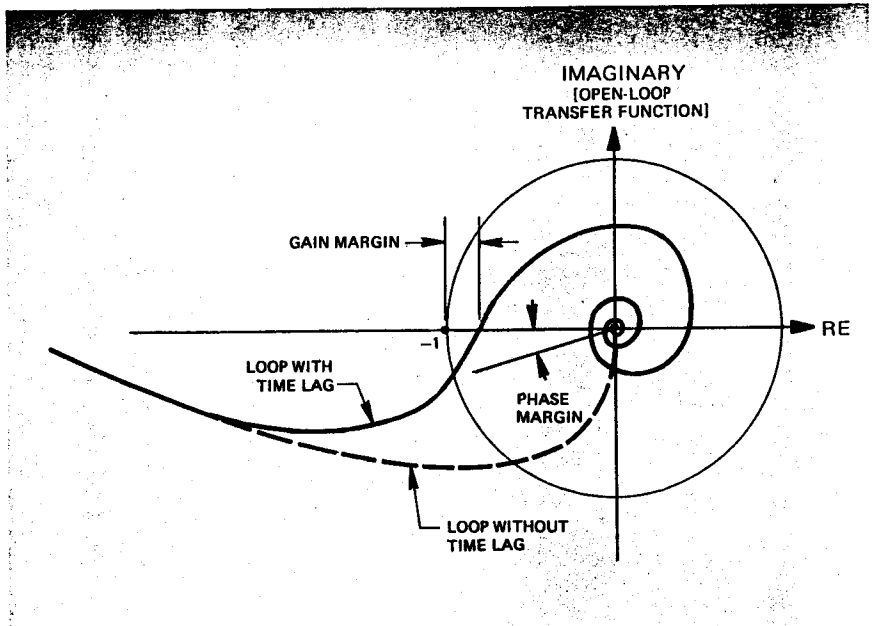
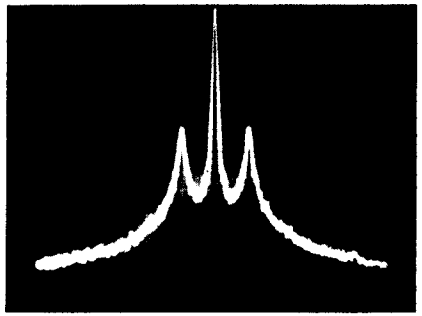


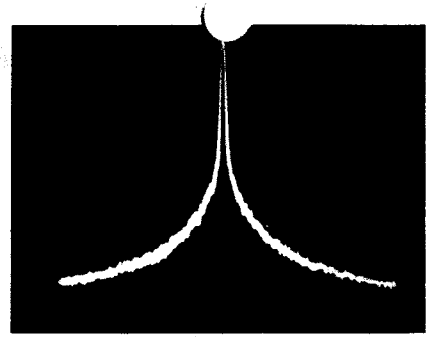

**Figure 8. This Nyquist Plot shows more clearly the effect of time delay. As the plot gets closer to the −1 point the closed loop system becomes less stable.**

*For a much more complete discussion, see B. C. Kuo's book *Automatic Control Systems.*





**9A. Horizontal — 20 kHz/Div.
Vertical — 10 dB/Div.
Center — 8.0 GHz**

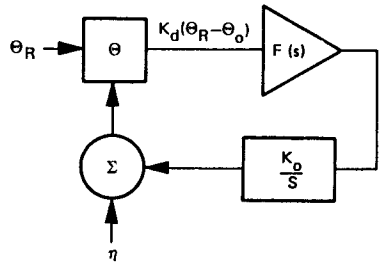


**9B. Horizontal — 20 kHz/Div.
Vertical — 10 dB/Div.
Center — 8.0 GHz**

**Figure 9. Noise peaking at about 20 kHz away from the carrier can be seen in 9A, while a slight modification of the design parameters eliminates the problem in 9B.**

## Phase Noise Peaking in PLL's

By beginning with the basic model of the PLL, as shown in Figure 3, noise sources and the behavior of PLL's in the presence of noise may be described. It can be seen that the noise from the phase detector and loop filter will modulate the VCO's output phase and that equivalent noise sources may be moved to the output of the VCO. The total noise at the output of the VCO is, therefore, the sum of the phase detector and loop filter equivalent sources plus the noise added by the VCO itself. This yields a noise model as shown in Figure A.




**A. Noise model for a PLL.**

The loop equation is now given by

$$\Theta_o = \eta + \frac{K_o}{s}[F(s)\, K_d\, (\Theta_R - \Theta_o)]$$

or, rearranging and collecting terms,

$$\Theta_o = \frac{\Theta_R K_o K_d F(s) + s\eta}{S + K_o K_d F(s)}$$

Looking at a high-gain second-order loop with

$$F(s) = K_f \frac{(s+a)}{s}$$

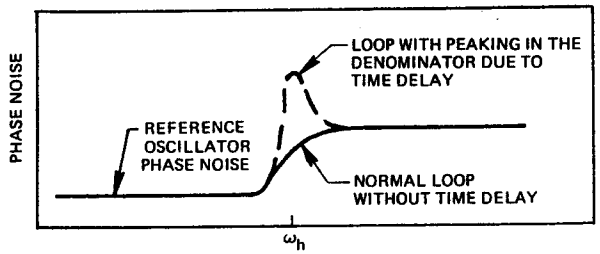
the expression for the output phase will be

$$\Theta_o = \frac{\Theta_R K_o K_d K_f (s+a) + s^2\eta}{s^2 + K_o K_d K_f s + K_o K_d K_f a}.$$

The term involving the noise, $\eta$, is a second-order high-pass function with a cut-off frequency, $\omega_h$, equal to the loop bandwidth. This means that any components of $\eta$ which are outside of the loop bandwidth will be transferred directly to $\Theta_o$. In other words, when one looks at the VCO's noise spectrum at offsets (from the carrier) greater than the loop bandwidth, the VCO will have the same characteristics as an unlocked VCO driven by the noise of the phase detector and loop filter.

If the denominator of the expression for $\Theta_o$ is modified to include the first-order effects of the transportation lag, it becomes

$$\Theta_o = \frac{\Theta_R\, K_o K_d K_f\, (s+a) + s^2\eta + \tau s^3 \eta}{\tau s^3 + s^2 + K_o K_d K_f s + K_o K_d K_f a}$$




**B. Effect of peaking due to time delay assuming $\eta$ is "white" noise.**

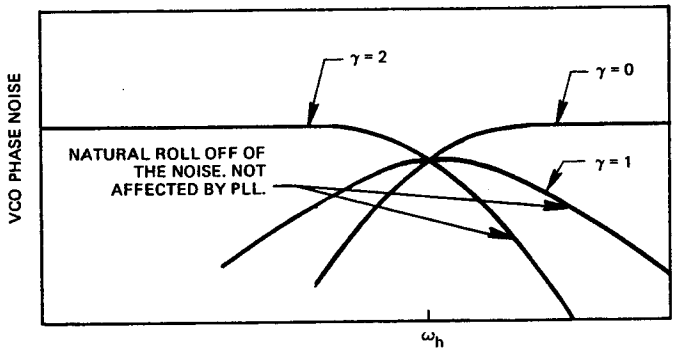
and peaking of the denominator will affect the noise as shown in Figure B.

Figure B assumes that $\eta$ is "white" noise. In general, this will not be the case, so it is of interest to see how the shape of the additive noise, $\eta$, affects the shape of the output phase noise spectrum. Assuming that

$$\eta = \frac{W}{s^{\gamma}},$$

a family of plots as $\gamma$ is varied may be made. This is shown in Figure C.

For $\gamma \geq 2$, a second-order PLL will not be able to pull the noise down to the level of the reference oscillator noise. Also, the curves of Figure C consider W as being constant in each case.




**C. Noise behavior of an ideal (no time delay) PLL.**

Since good noise performance is one of the primary reasons that make PLL's desirable, such noise peaking is to be avoided in the design stage if possible. To analyze the problem, it is helpful to observe the first-order effects of time delay. To begin, $e^{-s\tau}$ can be approximated as

$$e^{-s\tau} = \frac{1}{1 + s\tau + \frac{s^2\tau^2}{2!} + \ldots} \simeq \frac{1}{1 + s\tau}.$$



Substituting this first-order delay block into the block diagram of Figure 3 results in a loop transfer function of

$$T(s) = \frac{K_o K_d K_s (s + a)}{\tau s^3 + s^2 + K_o K_d K_f s + K_o K_d K_f a}$$

when

$$F(s) = \frac{K_f (s + a)}{s}$$ (High gain second-order loop)

The effect of the $\tau s^3$ term is most clearly seen in the root locus plot of Figure 10. The root locus shows the movement of the poles of T (s) as $\tau$ is varied from zero to infinity. At $\tau$ = o, the poles are as calculated by the ideal (no time delay) loop equations. As $\tau$ increases, however, the poles move toward the right half plane.

Because of the way in which the first-order effects of time delay move the poles of the closed-loop system,

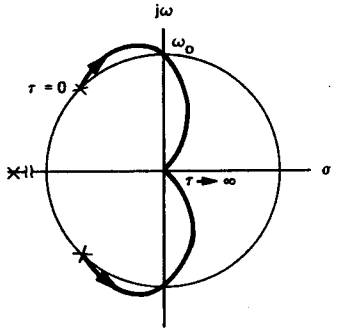



**Figure 10. The first-order effects of time delay (transportation lag) may be seen in this root-locus plot. This shows the movement of the poles as $\tau$ is varied from zero to ∞. Naturally, the first order approximation is only valid around $\tau$=0.**

the logical question to ask is, "How should the design parameters ($\omega_n$ and $\delta$) be adjusted so that the closed-loop system behavior does not have peaking?" One of the simplest ways to approach this problem is to require that the two complex poles of the closed-loop system be located where they would be without any time delay in the loop. For example, if one wanted $\delta$ = .707, the desired pole position would be at an angle of 45° to the negative real axis and at a radius of $\omega_n$. The closed-loop system would be adjusted so that the actual system poles would be at the same location. In general, this would result in a response for the closed-loop system, which rolls off slightly faster than a maximumly flat system. With this restraint, Figure 11 gives the correction factors for the design parameters, $\omega_n$ and $\delta$, as a function of $\omega_n\tau$ (the desired natural frequency multiplied by the time delay).

The following example will clarify this procedure: A PLL is desired to have a natural frequency of $\omega_n$ = 3 x $10^4$ rad/sec and a damping of $\delta$ = .707, and the loop has 5 $\mu$ seconds of time delay. Since $\omega_n\tau$ = .15, the correction factors are read as $\omega_n'$ (the design parameter) = .89$\omega_n$ = 2.67 x $10^4$ rad/sec and $\delta'$ = 1.25$\delta$ = .883. The loop filter is then designed using $\omega_n'$ and $\delta'$. Figure 11 is only valid for high-gain, second-order loops.

The curve of Figure 11 is also useful to compensate for the effects of extra poles in the loop filter, such as the far-out poles in the op amp, or the pole caused by the op amp running out of high-frequency gain. An example of this might be a design that calls for an AC gain, $K_f$, of 10 and an LM 101 as the op amp. The loop filter will have an "extra" pole at about 100 kHz, which would not show up when designed using the ideal (infinite gain) op amp. This pole would translate to an extra 800 nanoseconds ($1/\omega_p$) of time delay in the loop.

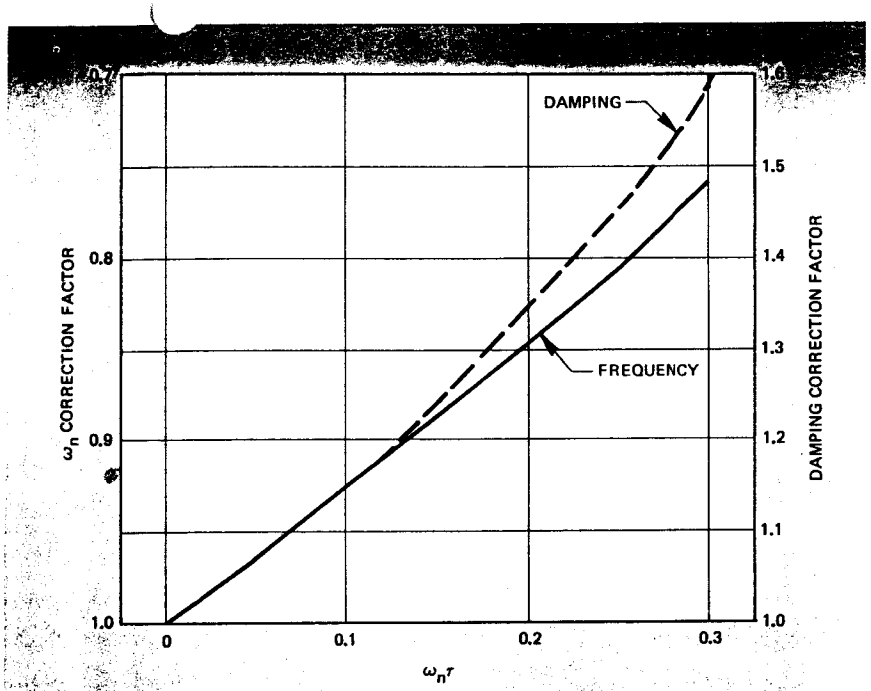



**Figure 11. Phase lock loop design parameter correction factors as a function of time delay.**

## Conclusion

This article was written with the intention of bringing to light a common problem encountered in phase-locked loops. By looking at the problem in several ways (phase and gain margin, Bode Plot, Nyquist Plot and root locus) it is hoped that it will give designers more of an intuitive feel for PLL behavior and how to cope with it. This, coupled with at least a first-order correction scheme, should save time as well as frustration.



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Dr. Wetenkamp is currently assigned to the Watkins-Johnson Company Amplifier and Mixer Section of the Solid State Division, where he is responsible for the design and development of thin-film microwave mixers.

Prior to joining the Solid State Division, Dr. Wetenkamp was assigned to the Frequency Synthesizer Section of the SSE Division, Systems Group. There, he was responsible for research and development leading to improved microwave frequency synthesizer systems and sub-systems. As Project Engineer, he was responsible for the timely and successful completion of contracted projects assigned to him.

Before joining Watkins-Johnson Company, Dr. Wetenkamp was employed as a research assistant at the coordinated Science Laboratory at the University of Illinois, where he completed research for his PhD. His doctoral thesis dealt with the use of multiple-loop feedback techniques in reducing circuit sensitivity to parameter variations.

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